

SIDNEY NEIL

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FPGA / Hardware Engineering · High-Speed PCB Design · Embedded Systems · HW/SW Co-design

PROFILE

Electrical and Computer Engineering student with demonstrated expertise in latency-critical hardware design — from high-speed PCB layout and signal integrity analysis through to FPGA synthesis, timing closure, and embedded Linux bring-up. Proven ability to deliver under extreme time pressure (international hackathon, 1st place). Seeking to apply low-level hardware and HW/SW co-design skills to FPGA infrastructure in a high-frequency trading environment.

CORE COMPETENCIES

FPGA & Digital Design: Verilog/SystemVerilog, RTL synthesis & timing closure, pipelining, clock domain crossing, DMA, I2S, SPI, UART, PCIe PHY layer

High-Speed PCB: Differential pair routing, controlled impedance (50 Ω / 100 Ω), length matching, PCIe Gen 3 (8 GT/s), M.2 form factor, stack-up design, SI/PI fundamentals

Embedded Systems: STM32, Yocto Linux (build, BSP, device tree), bare-metal C, DMA-driven peripherals, hardware bring-up & debug (oscilloscope, logic analyser, JTAG)

HW/SW Co-design & Tooling: Python (NumPy, Pandas, TensorFlow), React Native, Flask — used to build automated test harnesses and data-processing tools that validate hardware behaviour

Tools: KiCad / Altium, Vivado / Quartus, PSpice, MATLAB/Simulink, Git, TIA Portal (Siemens)

EXPERIENCE

Hardware Engineering Intern · *Astute Systems · Brisbane, QLD* Nov 2025 – Present

- ▶ Designed multi-layer PCBs end-to-end — schematic capture, controlled-impedance stack-up, layout, and DFM review — reducing board respins through rigorous pre-layout signal integrity analysis.
- ▶ Compiled and customised **Yocto Linux builds** for embedded ARM targets, including BSP porting, device tree authoring, and kernel driver configuration.
- ▶ Debugged hardware bring-up issues using oscilloscope, logic analyser, and JTAG; systematically isolated faults at the PCB, firmware, and driver levels to accelerate time-to-functional.

Founder & Lead Developer · *FitMatch* Jan 2026 – Present

- ▶ Architected and shipped a React Native iOS application end-to-end; demonstrates full-stack ownership and the same systems-thinking applied to hardware projects.

Junior ML Developer / Data Analyst · *Catalytics Data International* Sep 2024 – May 2025

- ▶ Engineered a **computer vision pipeline** in Python to automate catalog ad-block extraction, eliminating manual processing and improving throughput by an order of magnitude — the same data-pipeline discipline applied to hardware verification automation.
- ▶ Preprocessed large datasets using Pandas to enforce data integrity for downstream ML models.

New Colombo Plan Scholar · *Dalian Neusoft University of Information · China* Jun – Jul 2025

- ▶ Designed, prototyped, and demoed an AI-powered B2B SaaS platform in under four weeks; reinforced rapid iteration and cross-functional delivery under hard deadlines.

KEY PROJECTS

M.2 Ultra-Low Latency Serial-to-PCIe Conversion Board · *Lead Designer*

- ▶ Designing an M.2 2280 form-factor board targeting **PCIe Gen 3 ×1 (8 GT/s)** — the same physical-layer standard underpinning NIC and FPGA accelerator cards used in HFT infrastructure.
- ▶ Executing full SI workflow: differential pair length matching to **<±5 mil**, 100 Ω ±10% controlled impedance, via stub minimisation, and reference plane continuity across all high-speed nets.

- ▶ Integrating an FPGA for real-time serial protocol parsing and **sub-microsecond** PCIe transaction forwarding; targeting $F_{max} > 200$ MHz on the data path.
- ▶ Validating SI performance against PCIe Gen 3 spec using eye-diagram simulation; physical bring-up to follow with TDR and protocol analyser.

UAV Audio Recording & Real-Time DSP System · *Thesis Project*

- ▶ Engineered a **hard real-time** audio capture pipeline on STM32: I2S peripheral clocked at 48 kHz, double-buffered DMA transfers to eliminate any capture gap, deterministic interrupt latency $< 1 \mu s$.
- ▶ Implemented a fixed-point **FFT on Cortex-M4** using CMSIS-DSP; optimised for minimal clock-cycle count per bin to sustain continuous 1024-point transforms within a single DMA buffer period (~21 ms).
- ▶ Validated timing correctness with logic analyser captures on DMA half-complete and complete IRQ lines; confirmed zero-overflow operation under worst-case UAV vibration interference.
- ▶ Directly applicable to FPGA DSP blocks: the same fixed-point pipeline discipline maps to Xilinx DSP48 slices and latency-budget analysis.

International AI Hackathon — Bangkok · **1st Place (team of 4)**

- ▶ Solved a complex, open-ended geospatial prediction problem **under 24-hour competition pressure** — ingested 15 years of government flood records, engineered features, trained an ensemble model (TensorFlow + scikit-learn), and deployed a live map with email-alert system.
- ▶ Outperformed Google's public flood-forecast baseline by **75%** on held-out test data — result driven by feature engineering discipline, not model complexity.
- ▶ Demonstrates the rapid problem decomposition, clean architecture under pressure, and quantitative validation mindset expected in production trading infrastructure.

TPMania Arcade Console · *Embedded Systems Design*

- ▶ Designed a **DAC audio pipeline** on STM32L4 using I2S + DMA from SD card storage; achieved clean ± 1 V output with no CPU intervention during playback — freeing cycles for game logic.
- ▶ Integrated OLED (SPI), LED matrix, and debounced GPIO inputs; all peripherals driven via interrupt/DMA to maintain < 1 ms input latency.

Autonomous Micromouse · **UQ MARS Competition — 2nd Place**

- ▶ Sole designer and programmer: integrated IR sensor array, MPU6500 IMU, DC motor drivers, and Arduino Uno; implemented DFS maze-solving algorithm with real-time heading correction via gyroscope feedback.

EDUCATION

B.Eng — Electrical & Electronics Engineering · *The University of Queensland* Expected Dec 2026

Relevant Coursework: VLSI Design, Digital System Design, Analog & Digital Electronics, Signal Processing, Microelectronics, Control Systems, Circuit Design & Analysis